Express Mailing Label No. EV 382 941 301 US

PATENT APPLICATION
Docket No. 15436.259.1

UNITED STATES PATENT APPLICATION

of

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for

SYSTEMS AND METHODS FOR FABRICATING PRINTED CIRCUIT BOARDS

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SYSTEMS AND METHODS FOR FABRICATING PRINTED CIRCUIT BOARDS

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims the benefit of U.S. Provisional Patent Application No. 60/483,702 filed June 30, 2003, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The Field of the Invention

[002] The present invention generally relates to printed circuit boards (PCBs). More particularly, the present invention relates to systems and methods for fabricating printed circuit boards and more specifically to systems and methods for plating traces on PCBs.

The Relevant Technology

[003] An integral component of many electrical and optical devices is a multi-layer printed circuit board (PCB). PCBs are used, for example, to route signals and provide connections to various electrical and/or optical components. During plating, which is one of the steps that occurs during the fabrication of a PCB for example, some or all of the traces, vias, pads, etc., are plated with hard gold. Plating ensures that the PCB can make a solid electrical connection and strengthens the electrical integrity of the PCB. Usually, all features of the PCB requiring plating are plated at the same time.

[004] The typical plating process involves shorting all the contact pads by connecting them to small traces, which extend off the front edge of the PCB. The small traces then connect to a plating bar and a voltage is applied. By connecting all of the

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traces to a plating bar, all of the signal paths requiring plating in the PCB form a single conductive path. By applying a voltage, the resulting current electronically plates the gold on to the contact pads. In other words, all necessary signal paths are plated with hard gold at the same time. After the plating process is complete, the traces used to plate the appropriate portions of the PCB are cut at the front edge of the PCB, thus eliminating the short between the contact pads. One of the problems with this process is that small traces that extend from the contact pads to the front edge of the PCB remain on the PCB.

[005] This problem is illustrated in Figure 1 where the traces used to plate the contact pads (and other traces, signals, vias, etc. of the PCB) remain after the PCB has been routed to a final form factor. In Figure 1, the contact pads 102 provide electrical access to the signal or conductive paths of the PCB 100. As previously described during the plating process, the traces 104 were formed and connected to a plating bar (not shown). Thus, the PCB 100 illustrates the traces 104 that were used to plate the contact pads 102 and other conductive paths of the PCB 100. Note that Figure 1 illustrates the contact pads of the PCB 100, but it is understood that the other conductive paths that are connected with the contact pads are also plated.

[006] Unfortunately, the traces 104 are in the area 106 between a front edge 103 of the PCB and the contact pads 102. The presence of the small traces 104 in the area 106 of the PCB 100 may violate certain standards. In particular, the traces 104 may violate the GBIC/MSA standard. This standard requires that the contact pads within a GBIC/MSA device be set back from the PCB edge. Other small form factor pluggable standards (GBIC, SFP, XFP) may have similar requirements.

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[007] Another problem produced by the typical plating process is that it may interfere with high-speed traces, which are connected to certain contact pads. The purpose of the high-speed traces is to send high-speed data through the PCB. To achieve this purpose, high-speed traces involve careful balancing of impedances. The small traces that extend from the contact pads to the edge of the PCB disrupt this balance and reduce the ability of the high speed traces to effectively transfer data at high speeds. Cutting the small traces produces large stubs at the edge of the PCB, which do not affect performance of low speed traces but create interference among the high-speed traces and adversely affect the performance of these high-speed lines.

[008] Previous attempts to improve the plating process and eliminate the extension of small traces to the front edge of the PCB have been unsatisfactory. For example, etching, a technique employed to remove the small traces 104 from the area 106 of the PCB after the plating process, is expensive for use in low-cost transceiver modules.

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BRIEF SUMMARY OF THE INVENTION

[009] These and other limitations are overcome by the present invention which relates to systems and methods for plating a printed circuit board. In one embodiment, traces are formed from the contact pads to the side edges of the printed circuit board. This ensures that an area between the contact pads and the front edge of the printed circuit board does not have residual traces. The traces from the contact pads to the side edges of the printed circuit board may be formed on internal layers and/or external layers of the printed circuit board. Some traces may have a portion on an external layer of the printed circuit board that is connected through a via to a portion of the trace on an internal layer of the printed circuit board.

[010] After the traces are formed, the contact pads (as well as the conductive paths of the printed circuit board) are plated by connecting the traces to a plating bar and applying a voltage or current. After the contact pads are plated, the plating bar is removed and the link between the separate contact pads (or conductive paths) is broken and the printed circuit board is plated. The link can be broken, for example, by routing the printed circuit board to a final form factor.

[011] In another embodiment, some of the conductive paths may be transmission lines where it is undesirable to have long stubs. The long stub is eliminated by drilling a hole through the trace used to plate the transmission line at a point close to the transmission line. This typically leaves a negligibly short stub that does not impact the transmission line. Also, the transmission line can be plated by forming a trace from the transmission line to a nearby conductive path (such as a via). This enables the transmission line to be plated without forming a relatively long trace from the transmission line to the side edge of the printed circuit board. A hole is then drilled or

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otherwise formed in this trace to reduce a length of the stub and to electrically isolate the transmission line from other conductive paths of the printed circuit board.

[012] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by the practice of the invention. The features and advantages of the invention may be realized and obtained by means of the instruments and combinations particularly pointed out in the appended claims. These and other features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

[013] To further clarify the above and other advantages and features of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[014] Figure 1 illustrates a top view of a PCB having traces that extend from a front edge of the PCB to the contact pads of the PCB;

[015] Figure 2 illustrates a view of the top external layer of a PCB that is plated without leaving traces between the edge of the PCB and the contact pads;

[016] Figure 3 illustrates a top view of a PCB where a high speed transmission line is plated;

[017] Figure 4 is a magnified view of a portion of the PCB in Figure 3 and illustrates plated transmission lines; and

[018] Figure 5 illustrates a board that includes multiple PCBs that are all plated at the same time.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[019] The present invention relates to systems and methods for fabricating printed circuit boards (PCBs) and more particularly to plating conductive paths including contact pads of PCBs. The present invention has the advantage of eliminating the small plated traces that extend to the front edge of a PCB from the contact pads and also of minimizing the stub length on high speed transmission lines on the PCB that are formed during the conventional plating process.

[020] To eliminate the small traces extending to the front edge of the PCB, the contact pads on the external layer are connected to traces on an internal layer(s) of the PCB. The external contact pads are connected to the internal traces through vias, small pathways running between the layers of the PCB. The vias are formed through the multi-layer PCB by a drilling operation performed before the plating process. The traces lead to the sides of the PCB instead of to the front edge of the PCB. During the plating process metal is deposited through the vias onto each layer of the PCB.

[021] As indicated, the traces on the internal layer(s) are routed to the sides of the PCB where are attached to an external plating bar. The external plating bar serves to short all the connections from the traces together at one central point. In this example, the PCB includes a single conductive path. Once the traces are attached to the plating bar, a current or voltage is used to deposit the gold onto the contact pads, conductive paths, vias, traces, and the like.

[022] Plating the high speed traces or transmission lines on a PCB can result in problems as the traces used to plate the high speed traces may form long stubs that interfere with the impedance of the high speed traces. In one embodiment, thin traces connect the high-speed traces to ground pins located on the PCB near the high-speed

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traces and thus create a short during the plating process between the ground pins and the high-speed traces. After completion of the plating process, a hole is drilled through the thin trace, thus removing the short. The hole leaves a very short stub that will not adversely affect performance of the high-speed trace, unlike the large stubs created when a connecting trace is routed to the side of the PCB.

[023] The present invention is described in terms of a PCB used, for example, in Gigabit Interface Converters ("GBIC") devices such as GBIC optical transceivers. One of skill in the art, however, can appreciate that the present invention relates generally to PCBs and is not limited to PCBs used in specific devices. Embodiments of the present invention thus extend to PCBs that can be implemented, for example, in SFP, XFP devices, and the like.

[024] As illustrated in Figure 1, current plating technologies leave traces 104 that are undesirable in some instances. Specifically, the plated traces 104 may violate the specifications of some standards such as the GBIC/MSA standard. Figure 2 illustrates a PCB fabricated in accordance with one embodiment of the present invention that eliminates the traces 104 as illustrated in Figure 1.

[025] Figure 2 illustrates a PCB 200 that is defined by the outline 218. As illustrated, the area 224 between the contacts 220 and a front edge 221 of the PCB 200 does not include any traces such as the traces 104 illustrated in Figure 1. The contact pads 220 along with other conductive paths within and/or on the PCB 200 are typically plated with hard gold (or other suitable material). In this example, traces are used to form a single conductive path between the contact pads 220 and other conductive paths and a plating bar 202. The traces, illustrated as traces 210, 212, 214, 216, 204, 206, and

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208, lead from a conductive path on the PCB 200 to a side edge of the PCB 200. Usually, the traces are on an internal layer of the PCB 200.

[026] The traces 210, 212, 214, 216, 204, 206, and 208 do not lead to the front edge 221 of the PCB 200. For example, the trace 206 leads from a side edge of the PCB 200 to a via 252. This portion of the trace 206 is likely on an internal layer of the PCB 200. A trace from the via 252 to one of the contact pads 220 completes the trace. This portion of the trace 206 from the via 252 to the contact, however, may be on an external layer or on another internal layer of the PCB 200. Other contact pads 220 have a trace that can be followed to a side edge of the PCB 200. As previously stated, the portion of the trace from the contact pad to a via may be on an external layer of the PCB 200 while the remaining portion of the trace from the via to the side edge of the PCB is on an internal layer of the PCB. The vias are used to provide a connection from the external layer of the PCB to the internal layers of the PCB. In one embodiment, the traces 210, 212, 214, 216, 204, 206, and 208 can exist on different layers of the PCB 200. This often occurs in order to insure that the various conductive paths are electrically isolated when the PCB 200 is routed to the outline 218.

[027] The traces 210, 212, 214, 216, 204, 206, and 208, when connected with the plating bar 202, cause the contact pads, vias, signal paths, etc. on the PCB 200 to form a single conductive path in one embodiment. A current or voltage can then be used to plate all of the conductive paths at the same time. After the conductive paths such as the contact pads are plated, the PCB is cut or routed to a final outline (indicated by the outline 218). By cutting the PCB 200 to the outline 218 the connections between the traces 210, 212, 214, 216, 204, 206, and 208 is removed and the various conductive paths of the PCB 200 are electrically isolated.

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[028] Figure 3 illustrates another embodiment of the present invention that also relates to plating transmission lines or high speed traces. The PCB 300 in this example, includes transmission lines 320, 322, 324, and 326. Because transmission lines may be sensitive to impedances, it is undesirable to have long stubs. For example, if a trace is formed from the transmission line 322 over to a side edge of the PCB 300, then the trace would form a long stub and would remain attached to the transmission line 322 after the PCB was routed to a final form factor. This trace would be similar to the traces 210, 212, 214, 216, 204, 206, and 208 illustrated in Figure 2.

[029] As illustrated in Figure 3, a trace 370 is formed from a transmission line 322 to a nearby line or signal trace 321 that is not affected by longer stubs. In one embodiment, the trace 370 may connect to another signal such as a ground plane and the like. This is more clearly illustrated in Figure 4, which is an expanded view of a particular portion 350 of Figure 3. The process for plating the high speed transmission lines 320 and 324 begins by forming a trace to a nearby conductive path or signal. In this example, the transmission line 320 is connected with the contact 321 using a trace 370 and the transmission line 322 connects with a contact 323 using a trace 372. As illustrated and described in Figure 2, the particular pads 323 and 321 may be connected to a plating bar using another trace.

[030] In this example, the trace 370 is formed from the transmission line 320 to a via 376 either on a top layer of the PCB or on an internal layer of the PCB. The trace 377 connects to the trace 370 through the via 376 and the trace 377 connects to the contact 321. For this example, the traces illustrated in Figure 2 are not shown for clarity although they are present in order to plate all conductive paths of the PCB as previously

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described. Using the traces 372 and 370, the high speed transmission lines are plated during the plating process.

[031] After the plating process has been completed and the transmission lines are plated, a drilling process creates small holes 356 and 358 in the thin traces 370 and 372 respectively to disconnect the traces from the high speed transmission lines. After the drilling process is completed, short stubs 352 and 354 remain, but these short stubs do not adversely affect the integrity of the high-speed traces to which they are attached. By controlling the drilling process, the length of the short stubs 352 and 354 can be negligible.

[032] In contrast, plating the transmission lines using a trace as described with reference to Figure 2 leaves a long stub from the transmission line to the edge of the PCB. This long stub may have an adverse effect on the transmission line.

[033] In another embodiment, the transmission lines may be plated using traces as described with Figure 2 in combination with a drilling process that results in a short stub as described. In each embodiment, a short stub is left. The length of the stub, however can be controlled by drilling holes that are close to the transmission lines.

[034] In another embodiment, more that one PCB can be plated at the same time. Figure 5, for example, illustrates a plurality of PCB boards 500 that are all connected during the fabrication of the PCBs including the plating process. At a later stage of PCB fabrication, the PCB boards 500 are cut into separate PCB boards 502, 504, 506, and 508 by separating the individual PCB boards along the dashed lines 510, 512, and 514. A drilling process then forms holes such that the high speed transmission lines are not connected to long stubs that may adversely affect the transmission ability of the

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transmission lines. The drilling process may occur before the individual PCB are routed.

[035] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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